Group Report

1965-6

W. G. Schmidt
D. E. Chace

Design Aspects
of Minimal-Power
Digital Circuitry

9 February 1965

Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Lexington, Massachusetts

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

DESIGN ASPECTS OF MINIMAL-POWER DIGITAL CIRCUITRY

W. G. SCHMIDT

D. E. CHACE

Group 63

LEXINGTON   MASSACHUSETTS

ABSTRACT

Minimal-power digital circuitry, while a necessity for spacecraft operation, has advantages which apply to both space-borne and ground-based digital data processing.

This report is a compendium of some of the low-power digital circuit design efforts in which Lincoln Laboratory has been engaged for the past few years. These techniques have been employed in a number of scientific satellites and space probes; similar designs are to be used in the Lincoln Experimental Satellite (LES).

The report concludes with a discussion of the influence of new semi-conductor devices upon the minimal-power concept.

TABLE OF CONTENTS

DESIGN ASPECTS OF MINIMAL-POWER DIGITAL CIRCUITRY

I. Rationale of Minimal-Power Circuitry

To paraphrase an old but very true bromide, necessity is an excellent motivation. This seems to have been true in the case of low-power digital circuitry, interest in which has only been developed with the advent of space-craft systems and their associated highly-constrained power systems. Faced with the need for significant amounts of on-board data processing but limited by the available power, the digital systems engineers became increasingly anxious about a "bits per watt" figure-of-merit. This is particularly true of the scientific satellites which usually have limited solar-oriented geometries; this, in turn, limits the power generated in the solar panel arrays. The development of highly-efficient circuitry became a necessity.

The quest for minimal-power designs has several other exceptionally interesting aspects and these do not have implications for the spacecraft designer alone but, rather have broad meaning for _all_ future uses of electronics. The first, and certainly the foremost, is the reliability which such minimal power circuitry affords. It is well-known that the reliability of components is related to their internal stress levels (thermal, mechanical, etc.) and most of the failure rates are predicated upon the designed derating of the particular component. The reliability of those components which are employed at less than ten percent of their maximum rating is, to our knowledge, generally unknown because of tests necessary to ascertain the failure

rates must, to be of statistical significance, be exceptionally lengthy in time and incorporate very large sample sizes. It is not imprudent, however, to assume that components utilized at power levels which are 1×10^{-3} that of their maximum permissible power dissipation have, essentially, the reliability of a component on a shelf with no power applied. Any component failures which are caused must occur by reason of other stresses, probably mechanical or internal molecular changes caused by composition instabilities or radiation damage. Hence, circuitry designed for low-power dissipation insures lower failure rates. Intuitively, those components operating at the microwatt level should have reliabilities which are, at least, an order of magnitude better than milliwatt level circuitry, by reason of a three-order of magnitude reduction in thermal stressing.

In those situations in which the amount of power is fixed and in excess of what a well-designed low power system requires, the use of subsystem redundancy will bring substantial improvement in the reliability of the system. The amount of redundancy employed depends completely upon the uncommitted power remaining and the amount of space still remaining in the system. The coupling of the reliability of low-power circuitry to the redundancy techniques available yields a capability of developing spacecraft systems which have lifetimes compatible with the requirements of such long lifetime systems as communication satellites, navigational beacons, meterological monitors, etc. Since the replenishment rate is a function of the number of units in orbit and the lifetime of each unit, the doubling of the lifetime will have substantial savings in the number of reinsertions necessary to maintain an orbiting system.

Another aspect of minimal-power circuitry is the wide latitude the low thermal stressing affords the packaging engineer. Free-air cooling is more than sufficient and most of the thermal constraints relating to circuit encapsulation are removed. Even more interesting is the marriage of low-power circuit technology with the integrated circuit technology. While integrated circuits are small, they still have power dissipation in the ten to thirty milliwatt region. This is dictated by the resistance per square of the current state-of-art of deposited thin-films used as resistors and the masking technology of the semiconductor processing. Hence, the maximum number of circuits allowable to the cubic inch, under the constraint of fixed surface temperature rise, depends on the surface cooling mechanism and the power dissipation per circuit. It has been shown by Suran[1], that if a surface-to-ambient temperature differential of 20°C is an upper limit, only 20 circuits are allowable per cubic inch if each circuit dissipates 20 milliwatts; the material of the cube is considered to be germanium. The vacuum of space worsens the situation since heat may no longer be conducted away from its source. A three-order of magnitude reduction of power dissipation per element will allow a similar increase in packaging density to 20,000 circuits per cubic inch, which is approximately the theoretical maximum packaging density of which the current integrated circuit technology is capable. Hence, if integrated circuitry is to reach its theoretical packaging capabilities, the

---

1. J. Suran, "Circuit Considerations Relating to Microelectronics", Proc. IRE., Feb. 1961, pp. 420.

minimal-power circuit techniques must be developed to the limit.

There are two sidelights to this aspect of low-power circuitry which are of import to ground-based technology. The first is the elimination of any mechanical forced-air cooling system requirement on any large ground-based digital system; such air-cooling systems tend to have very high failure rates compared to the electronic systems they support, and are usually a limiting factor in overall system reliability. The second is that the more efficient use of integrated circuits will serve as the prelude to the implementation of the "microsystem" concepts being proposed today.

II. Minimal-Power Storage Circuitry

For purposes of this discussion there are two very broad areas into which static logic digital circuits may be divided: Storage elements, which primarily consist of flip-flops and the associated gates which enable them to function as counters, shift-registers, etc., and logical elements such as the circuits which perform various Boolean operations, e.g. NAND and NOR circuits. The first section of this report will consider various aspects of the design of minimal-power storage circuitry.

A. Standby Considerations

The workhorse of any digital system is invariably the flip-flop, the classical form of which is the Eccles-Jordan configuration of Figure 1.

In most designs the value of R_2 is considered insignificant compared to R_1 and, accordingly, the equivalent circuit for the side of the flip-flop which has its transistor off and output voltage positive is shown in Figure 2, with a worst-case loading.

If the minimum allowable voltage of V_{out}^1 is denoted as $\underline{V_{out}^1}$, then solving for R_1 yields

$$R_1 = \frac{R_L(E - \underline{V_{out}})}{\underline{V_{out}^1}} = \frac{R_L E}{\underline{V_{out}^1}} - R_L$$

$$= R_L \left[\frac{E}{\underline{V_{out}}} - 1 \right]$$

Note that if $\underline{V_{out}^1} = E/2$, $R_1 = R_L$ and the power dissipated in R_1 is

$$P_{dis} = \frac{E^2}{4R_1}$$

The worst case of loading when the transistor is on and saturated is shown in Figure 3. The transistor must then have sufficient current gain in the saturated state such that

$$I_c \cong \frac{E}{R_1 || R_L}$$

and the power now dissipated in R_1 is

$$P_{R_1} = \frac{E^2}{R_1}$$

If $R_1 = R_L$, and R_{sat} of the transistor is assumed constant, the power

dissipated in the transistor has increased by a factor of four.

From the foregoing it is evident that to minimize the power dissipation

within the flip-flop, a switch is needed in the place of R_1 such that when the

transistor is on, the switch is open and all the current being pulled by the

transistor is from the load. Conversely, when the transistor is off, the

switch should be closed, yielding the lowest possible output impedance from

the circuits as well as enabling the E+ to drop to V_{out}^1 in value. Another

advantage to be gained by this method is speed, since the loading capaci-

tance is always charged and discharged through a low impedance. The

implementation of this scheme is shown in Figure 4[2, 3].

Here we see that the switch used in place of R_1 is implemented with a

PNP transistor used in a switching mode. Note that all currents internal

to the flip-flop are base-drive currents, the values of which depend upon

three parameters;

    1. Load requirements

    2. Transistor current gain

    3. Transistor leakage currents

2. T. P. Bothwell and L. Koldoin, "A Bistable Symmetrical Switching Circuit," Proc. of National Electronics Conference, 1955, pp 655-667.
3. R. H. Baker, "Maximum-Efficiency Transistor Switching Circuits," MIT Lincoln Laboratory Technical Report No. 110, March 1956.

and it is these parameters which determine the minimum power dissipation of the flip-flop, some of which have been built and operated at 60 nanowatt levels, with three volt signal swings. The difficulty with operation at this level is simply that the internal impedances become so high that the circuits must be shielded from the normal laboratory environment. A flip-flop design which has proven itself to be extremely reliable in several systems built at Lincoln Laboratory is shown in Figure 5. It is designed for operation between $-30^{\circ}C$ and $+60^{\circ}C$, with full load being 100K (to +6 or ground) shunted by 200μμf. Turn-on and turn-off times of the circuit are typically less than 1.0μ sec. Dissipation, with a six volt swing, is less than 100μw. The resistor divider in the base drive of each transistor is utilized to provide noise protection for the circuit. Since the complementary transistor flip-flop tends to generate current pulses on the power buss at switching times, such protection is felt to be desirable for a good "system circuit".

B. Switching Considerations

While the saturated mode maximum-efficiency flip-flop described previously seems to be perfect for minimal-power storage, it does have some drawbacks when used at switching rates greater than about 3 kcps. particularly from the minimal-power viewpoint. A power profile of the flip-flop is shown in Figure 6. Note the great increase in power dissipation as the switching rate moves above 10 kcps. Why does this flip-flop, which is in minimal-power operation at low rates, consume inordinate amounts of power as the switching rates increase?

7

In order to provide an answer to this question, as well as an insight into the transient effects of transistor switching, it is convenient to use a charge analysis approach to study the transient times of the switched transistor. This is accomplished by attempting to determine the actual charge requirements of the transistor in its various regions of operation and calculating the time required to fulfill those charge requirements under the constraint of current source base drives. This type of analysis is particularly applicable to minimal-power circuitry because of the large base-drive resistor usually employed.

Let us study Figure 7 with switch, S_1, in the ground position, the emitter and collector junctions are biased off and only leakage currents, usually negligible, flow accross the junctions. When S_1 is thrown into the E+ position, no collector current flows for a while. The initial charge supplied through R_b is used to fulfill the charge requirements of the emitter and collector junction depletion layers. This charge requirement continues until the emitter junction becomes forward biased and begins emitting ($V_{bc} \cong 0.3$ volts). The quantity of charge which is supplied to the emitter junction depletion layer depends upon the initial biasing conditions and is called Q_E. Q_{CD} is the charge supplied to the collector depletion region and this obviously also depends upon the initial biasing condition as well as the collector supply voltage.

The transistor is now in the active region until such time as $V_{cb} = 0$, which is the edge of the saturated region. The charge requirements during this time period is the base gradient of charge, C_B, and the collector charge,

C_c. Since the rate of recombination of the charge in the base region still has not reached an equilibrium with respect to the base current, the transistor enters the saturation region more deeply. Q_{BX} is the excess charge which is a function of the current in excess of that required to saturate the transistor.

The transient times are now defined as approximately

$$t_{delay} = \frac{Q_E + Q_{cp}}{I_{B1}}$$

$$t_{rise} = \frac{Q_B + Q_c}{I_{B1}}$$

$$t_{storage} = \frac{Q_{BX}}{I_{B2}}$$

$$t_{full} = \frac{Q_B + Q_c}{I_{B2}}$$

For constant values of transient times, it is clear that the forward and reverse drive currents, so closely related to switching power dissipation, may be reduced only if the charge requirements are reduced. This can be accomplished in the circuit design and construction by several techniques

    a) Reduction of excessive back-biasing

    b) Use of smaller values of supply voltage

    c) Minimization of wiring capacitance on the leads.

In the device itself, advantage can be taken of the low thermal densities

encountered in minimal-power circuitry as well as the highly desirable low supply voltages. The transistor geometries may be made appreciably smaller, thereby causing substantial reductions in the charge requirments enabling faster switching at lower base drive currents. This approach is being realized by the semiconductor manufacturers and has lead to the Motorola development of the 2N3493, the first NPN designed for low-power switching. With C_{ib} and C_{ob} approximately 0.5 μμf, the charge requirements are extremely small. Some further work will improve the current gain characteristic of this transistor. Leakage currents are typically less than 50μμa.

If one returns to the complementary transistor flip-flop and applies a gating signal directly to the base of an off NPN, that transistor must drive the off PNP on and into saturation while turning the on NPN off. The recently turned on PNP must also now turn off the on PNP while keeping the initially triggered NPN in the ON state. The multiplicity of depletion region junction charge requirements which must be satisfied would ordinarily make this circuit very difficult to trigger. By the judicious use of speed-up capacitors, these charge requirements are more rapidly satisfied, but not without the price in power consumption, noise immunity, and repetition rate which such a technique involves. It is then seen that the reason for the excessive increase in switching power dissipation of the complementary transistor flip-flop is the circuit capacitances and the excess charge which must be cleared out of the on transistors before they can be turned off completely.

If the switching power of this circuit is to be reduced, several approaches can be used, including

10

a) Use of non-saturating techniques

b) Reduction of logic level swings

c) Use of small geometry transistors

One interesting circuit is that shown in Figure 8; the circuit is still a complementary transistor flip-flop but has been "stripped" of all internal resistors and capacitors such that the circuit operates at minimum supply voltages for such a configuration. In order to set up this circuit, connections S_1 and S_2 are open and R_1 and R_2 adjusted for the maximum allowable current with Q_1 and Q_3, and Q_2 and Q_4, respectively, on. When S_1 and S_2 are closed, the resultant circuit reverts to its bistable mode of operation. This circuit should be minimal power in standby and switching operation but the development of compatible gating circuitry is troublesome, primarily because of the complete loss of resistive isolation and the highly constrained voltage limits. Development of techniques to enable operation within these constraints is a challenge for the future.

C. Gating Considerations

The standard passive gate used for low-speed counting operations upon the complementary transistor flip-flop is shown in Figure 9 with a simplified flip-flop schematic connected to it. C_2 and R_3 form a differentiating network, which may be omitted in certain applications, while R_2 forms a drive regulating resistor; the positive-going edge of the input voltage wave form is formed into a current pulse and steered into the appropriate NPN base by the

$R_1 D_1$ network. The speed limitation imposed on this technique results from the value of the $R_1 C_1$ time constant.

Somewhat faster operation can be achieved by the use of the gating arrangement in Figure 10. This active gate is direct coupled to the NPN bases, which provide the voltage difference which steers the current for the switching action. Assume that Q_3 is on and Q_4 is off, which results in Q_5 off and Q_6 on. The voltage on the base of Q_1 is therefore, about 0.5 volts higher than the voltage on the base of Q_2. When the switch transistor, Q_7, is momentarily turned on, Q_1, (is turned on and) Q_5 on, and this starts the entire switchover process. The switching time of Q_3 is expedited by the base current being drawn by Q_1. For even faster circuits, the discharge time of R_1 and C_{out} of Q_7 may prove a hindrance to the development of very narrow current pulses. A complementary driver would then be added to the Q_7 circuit. The C_{ib} of Q_1 and Q_2 may require isolation from the bases of Q_3 and Q_4.

Operation in excess of 20 Mcps has been achieved by use of a tunnel diode and transistor gating system.

There are two variations on the low-speed gate which may be of interest. The first is a trailing-edge gate which operate on the PNP transistors of the flip-flop.[*] It is shown in Figure 11. The diode-steering network is identical to the low-speed gate shown previously but operated on the PNP's. Normally the inputs are high but when one is suddenly grounded, the negative going voltage pulse is coupled directly to the appropriate PNP for turn-on. A resistive isolator may be inserted as is used in the regular low-speed gate.

---

[*] This gate was developed by L. J. Travis and R. E. McMahon of Lincoln Lab.

A further variation of the basic configuration is the addition of components such that the gate may be used for counting and shifting as well. The counter shift-register gate is shown in Figure 12. It consists of a shifting gate, connected to the previous register stage, and a counting gate, commutated to the same stage. When the contents of the register are to be shifted, point D is grounded and the shift pulses applied to the shift input.

III. Minimal-Power Logic Circuitry

The standard gating configuration which has been used in digital systems is represented by the NAND circuit shown in Figure 13. In studying the output section of the circuit, we again notice that we have the same problem as was faced in the flip-flop design; it is again desirable to replace R_1 with a switching PNP. One configuration which would perhaps be tempting is shown in Figure 14. It should be noted, however, that this configuration will not operate satisfactorily when the inputs A and B are high. The symmetry of values of R_a and R_b will turn both the NPN and PNP on simultaneously, with the output level dependent upon the relative current gains of the transistors. In order to give this circuit a stable state when A and B are high, the values of the PNP drive resistors must be lowered, causing an increase in the power dissipation of the circuit.

In order to resolve this problem of maximum-efficiency logic circuitry and still remain with the very flexible design capabilities of diode-transistor logic, a universal logic circuit has been developed which performs the AND,

OR, NAND, or NOR functions, as well as having the capability of being used as a flip-flop. The circuit is shown in Figure 15.

When the circuit is to be used as an AND gate, the signals to be gated are connected to diodes D_1 and D_2. The only "ground rule" of the circuit is that the complements of these signals, invariably available, be connected to the other input section, in this case diodes D_3 and D_4. When the proper signal condition exists, Q_1 turns Q_4 on, Q_2 turns off and Q_3 turns off. The desired AND signal is available at $\overline{C}$, and the complementary NAND signal at C.

When the circuit is to be used as an OR gate, the signals to be gated are connected to the AND-NAND inputs. The OR signal is then available at C and its complementary NOR signal is available at $\overline{C}$.

By disconnecting the resistor R_D from E+ and tieing it to C, while connecting D_3 to C, the circuit becomes a flip-flop.

This circuit, which has acquired the name of "Schmoole," is a maximum-efficiency logic circuit which operated at the same power dissipation levels as the flip-flop. Its universal nature makes it an ideal logic element and one well-suited to those systems which are constrained to the use of only one type of logic circuit.

IV. Field-Effect Transistors

There has been increasing interest by circuit designers in field-effect transistors coupled with the improvements in these devices by the manufac-

14

turers. Such units would appear to be the answer to the problem of minimal-power switching since they have input resistance in the range of 10^{12} ohms and greater. One must bear in mind that utilization of such impedance levels indiscriminately would undoubtedly incur the same pick-up problems which plague the nanowatt circuitry cited previously.

There are indications that the switching power dissipated by these devices might be exorbitant since these devices typically require input voltage swings in excess of five volts, and the input capacitance of these units has been running typically about $5\mu\mu f$. As soon as the repetition rates increase, the charge requirements will make themselves known and the large signal swings will be costly. Experiments conducted with various types of field-effect units tend to confirm this. Enhancement types seem to have more promise in digital circuitry than depletion types but fabrication techniques must be improved in the future. The FET will probably make its first inroads in the low-power field in the regions of low and medium speed with this being hastened by the development of an N-channel enhancement device to complement the available P-channel enhancement types. Lowered voltage swings and much smaller geometries will have to be available before they can enter the high-speed low-power area.

The metallic-oxide semiconductor (MOS) enhancement mode field-effect transistor will be an extremely interesting digital logic device and should see considerable usage when a reliable corresponding N-channel device appears on the market, as well as improved process control. The fewer numbers of diffusion required by such a device should provide much higher yields than

are obtainable with standard planar transistors; prices of the MOS FET'S should reflect this.

The logic configurations possible using enhancement mode MOS FET'S are identical to those used for the DCTL circuitry, which was popular several years ago in logic systems. The chief disadvantages of DCTL involved base-current hogging in parallel-driven inputs, small fan-in on series elements, and very little noise immunity. Adapting MOS FET'S to this circuit approach eliminates these disadvantages since this device needs a large voltage swing (about four volts) to turn them on and they are basically voltage devices rather than current devices.

Figure 16 shows some logic configurations which may be used for combining P-channel units with standard transistors; the transistors being used as level discriminators and power amplifiers. R_1 is a current regulating resistor. When N-channel MOS FET'S are available and reliable enough, they can be substituted in these configurations, with discretion, for the NPN's The complimentary flip-flop would approximate the appearance of Figure 17. Resistive isolators might be needed to minimize the influence of the circuit capacitance.

V. Another Aspect

The selection of supply voltages for a low-power digital system is obviously very closely associated with the ultimate power dissipated by the system. In those systems in which the power busses are shared by the digital subsystem

with other subsystems, such as telemetry transmitters stabilization sub-systems, etc., the digital system may be required, for increased reliability and efficiency of the power converter, to utilize the voltage level dictated by these other subsystems. In cases wherein the digital portion is allotted its choice of buss voltage, diode-transistor logic will work conveniently to a three volt level, with transistor logic effective down to about 0.6 volt level. Tunnel diode logic can be utilized to a somewhat lower level, but requires larger currents to operate at its best.

It should be pointed out that the achievement of an absolute minimum of power dissipation, many times at substantial loss of circuit operation margins, is folly. The successful operation of an entire system is the goal of the systems designer, and the subsystem balance must be maintained. To incorporate a tight-margin microwatt digital unit, with a 100 milliwatt analog unit, coupled to a transmitter dissipating tens of watts with comparatively low efficiencies is an obvious imbalance and poor system design. Reliability should be the foremost consideration, and should not be sacrificed on the altar of "micropower".

VI. Conclusions

Design aspects of a variety of types of low-power circuitry have been presented, as well as some trends which are seen for the future. It is believed that long and more useful space vehicle lifetimes will result from increased emphasis on this aspect of digital systems design. The implications for

ground-based systems, particularly mobile digital systems, is similarly obvious. The coupling of recent advances in monolithic circuitry with low-power techniques should provide background for the microsystem technology of the future. Many of the circuits discussed previously are in the process of being integrated in multi-chip fashion (1/4" x 3/8" flat packs) for use in Lincoln Laboratory's Experimental Satellite program.
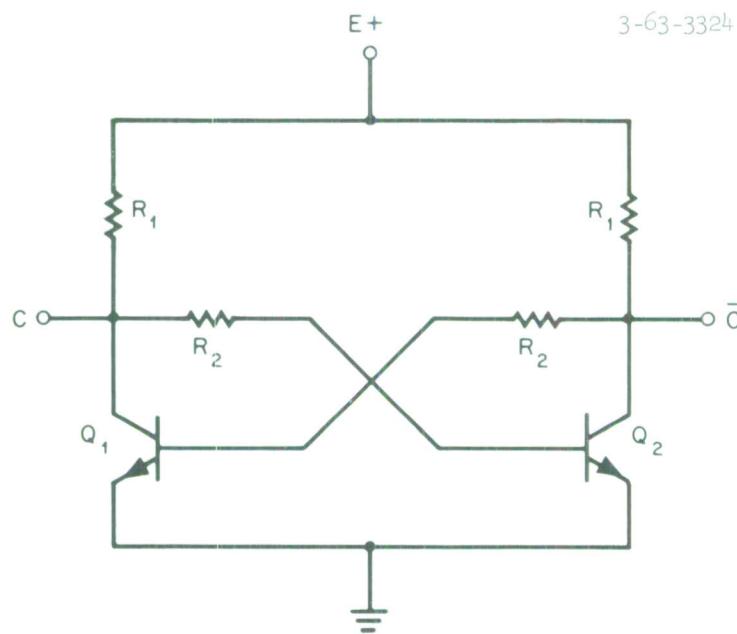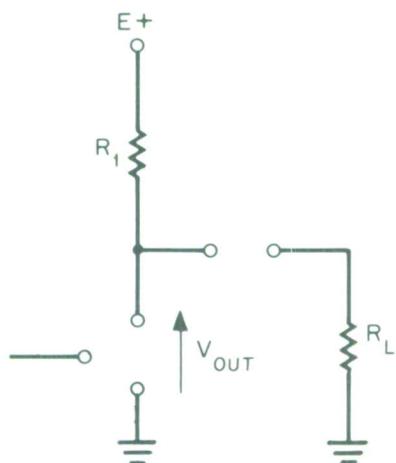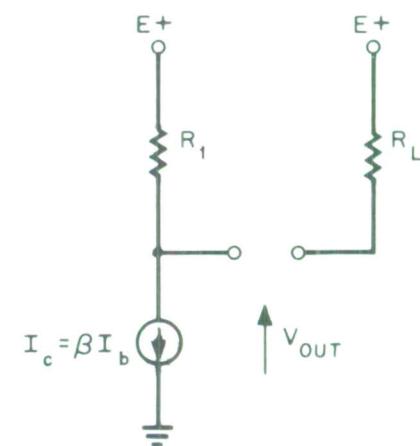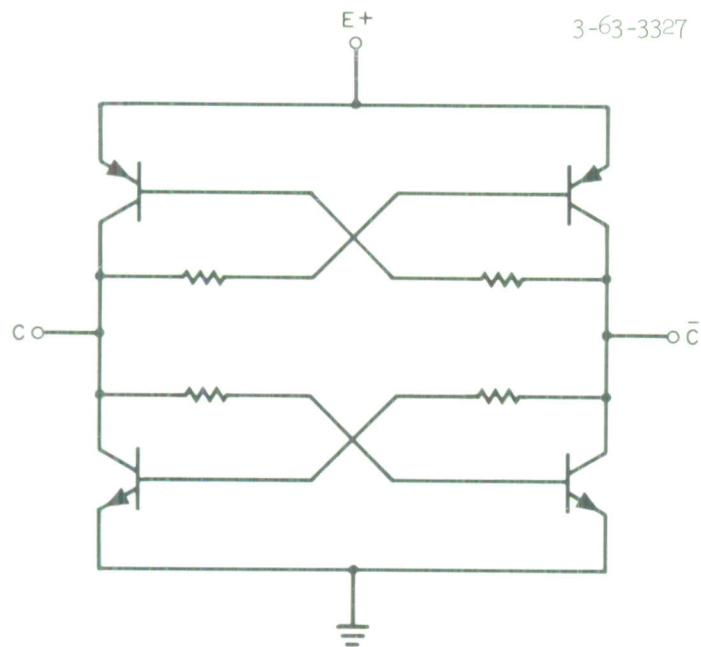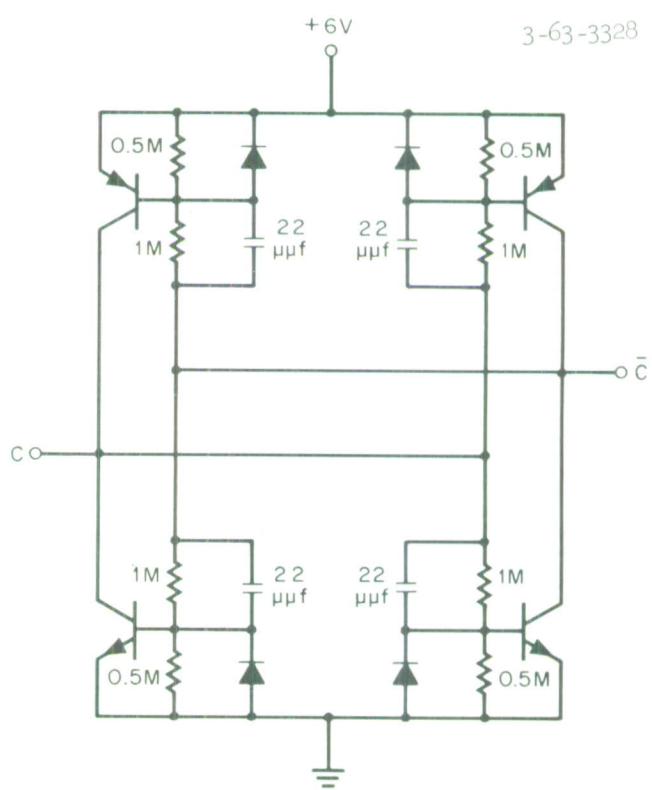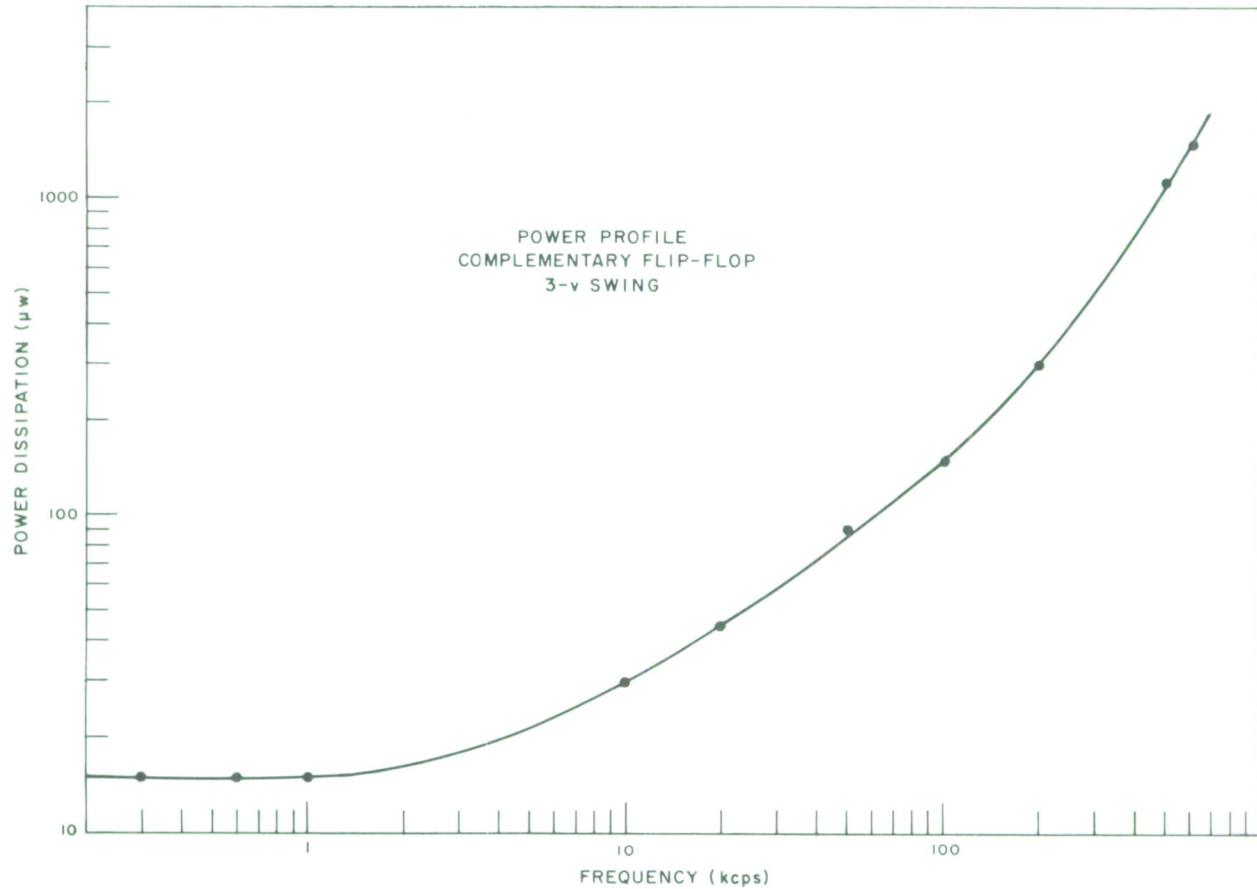
Fig. 1

Fig. 2

Fig. 3

E +

Fig. 4

+ 6V

0.5M

1M

22 μμf

22 μμf

1M

0.5M

C

C̄

1M

22 μμf

22 μμf

1M

0.5M

0.5M

Fig. 5

POWER PROFILE
COMPLEMENTARY FLIP-FLOP
3-v SWING

Fig. 6

3-63-3330

Fig. 7

Fig. 8

22
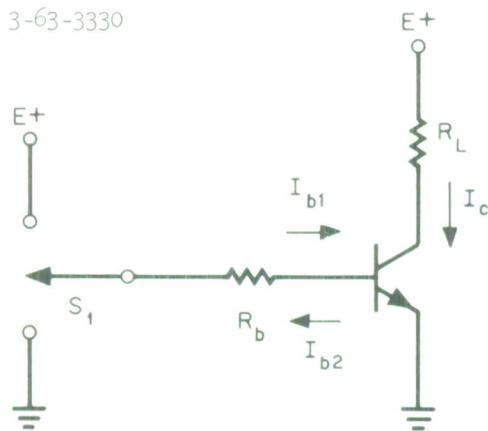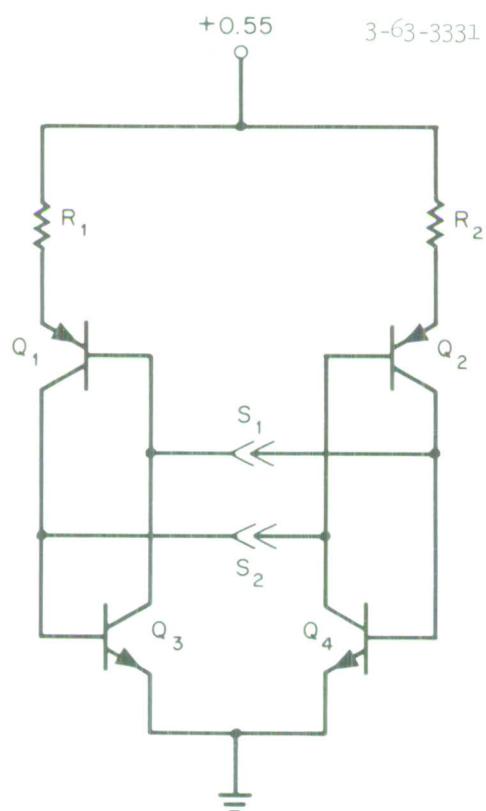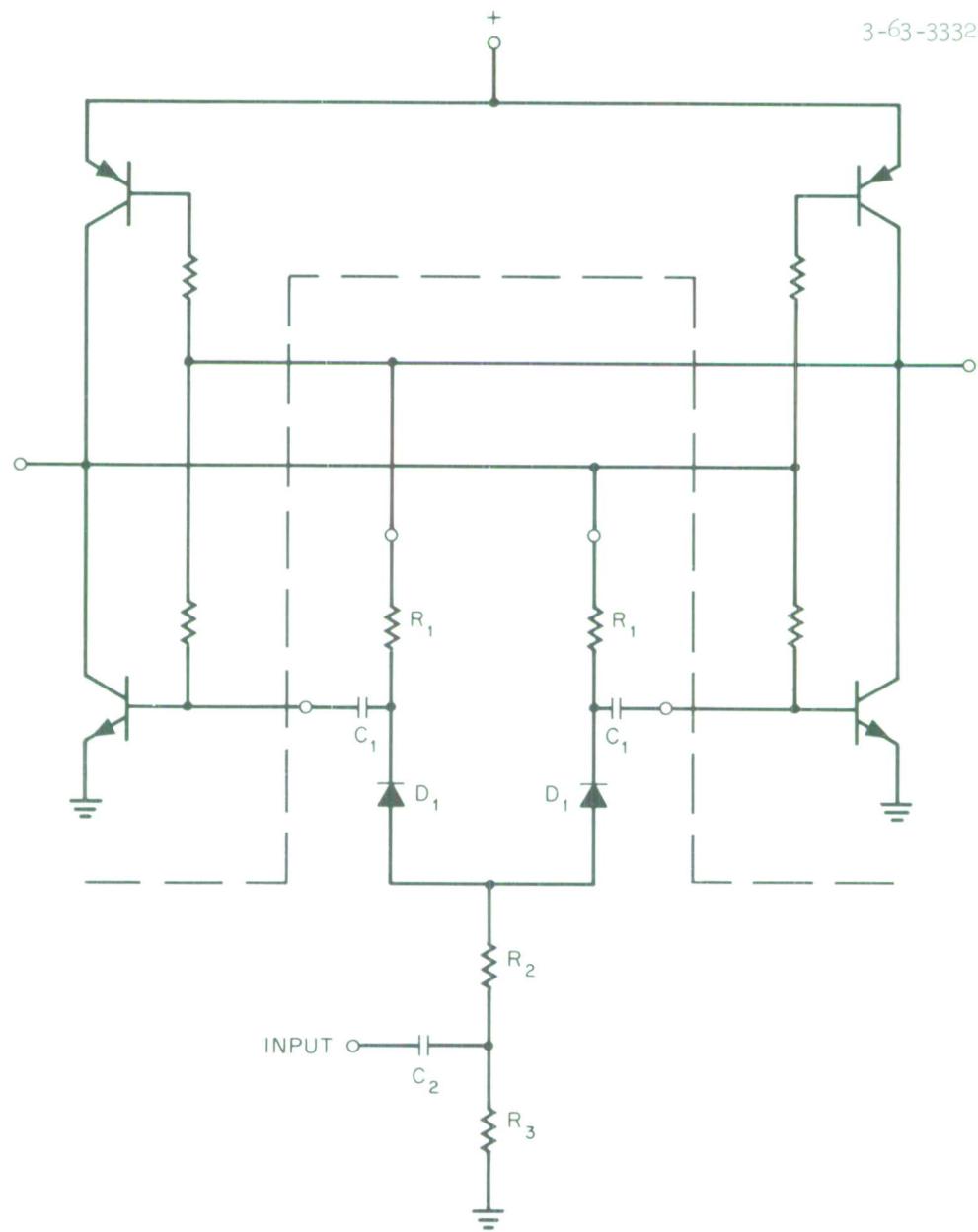
Fig. 9
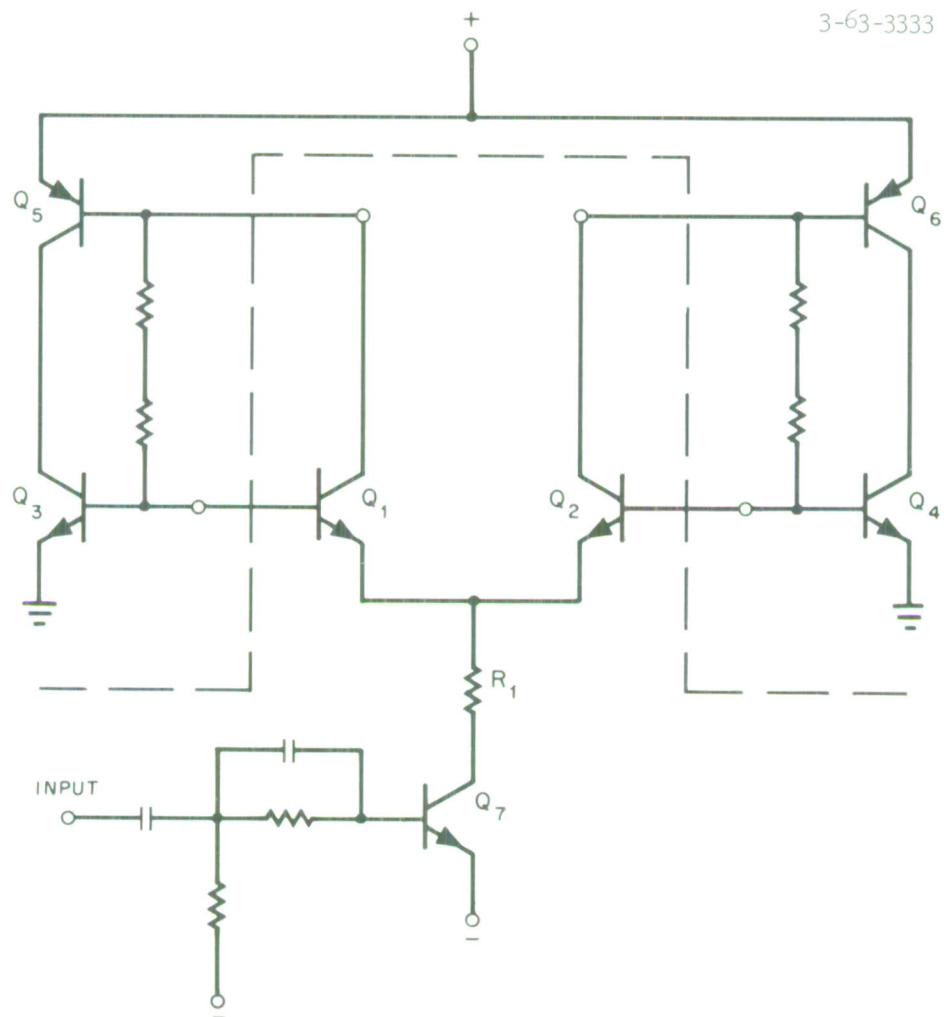
Fig. 10
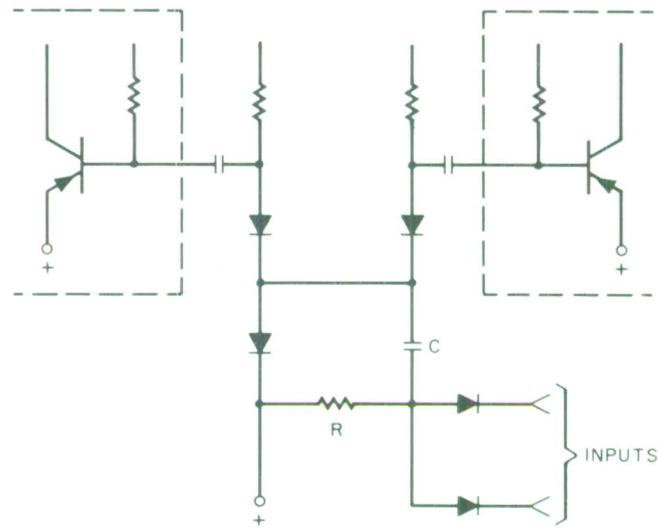
Fig. 11
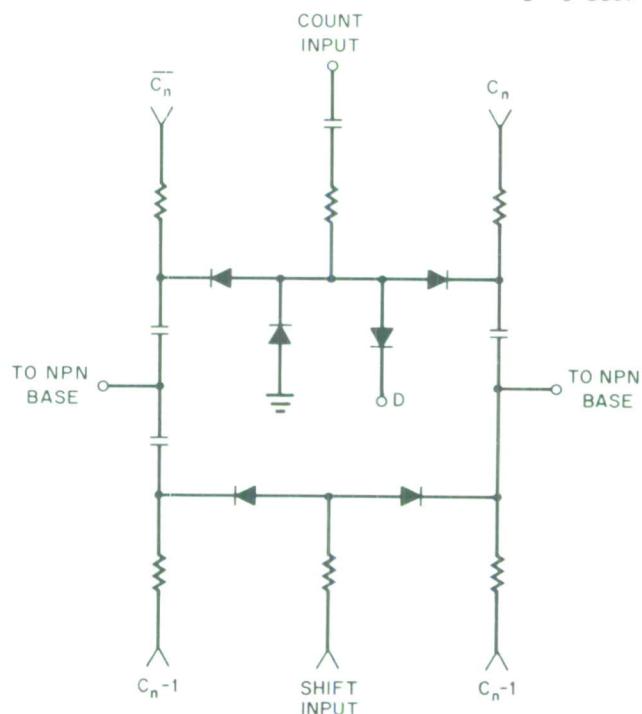
Fig. 12
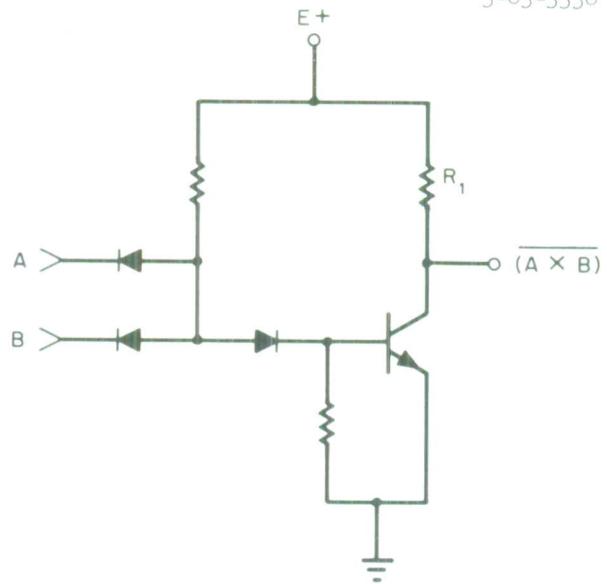
3-63-3336

Fig. 13

3-63-3337

Fig. 14

Fig. 15

Fig. 15

$$\overline{D} = \overline{A} + \overline{B} + \overline{C}$$
$$D = A \times B \times C$$
$$\underline{\underline{AND}}$$

$$\overline{D} = \overline{A} \times \overline{B} \times \overline{C}$$
$$D = A + B + C$$
$$\underline{\underline{OR}}$$

Fig. 16

28
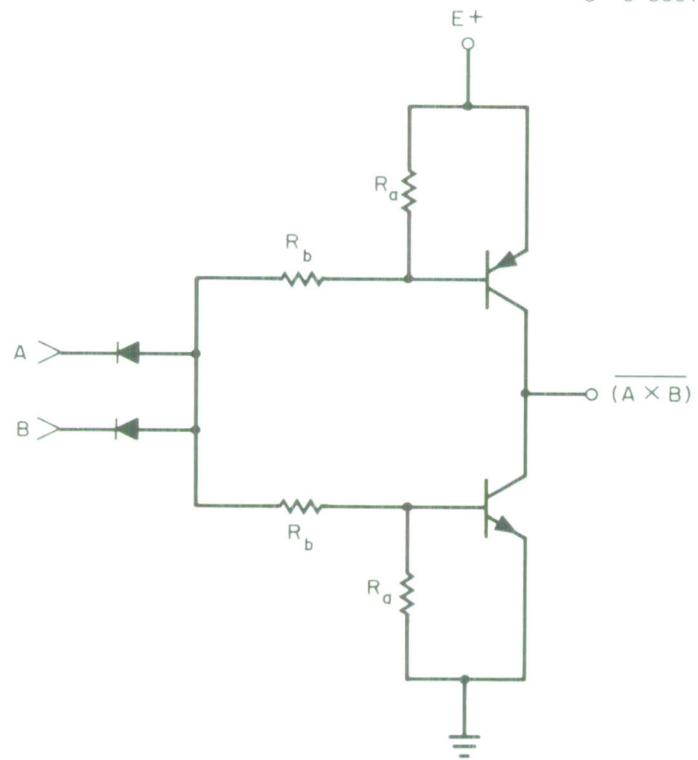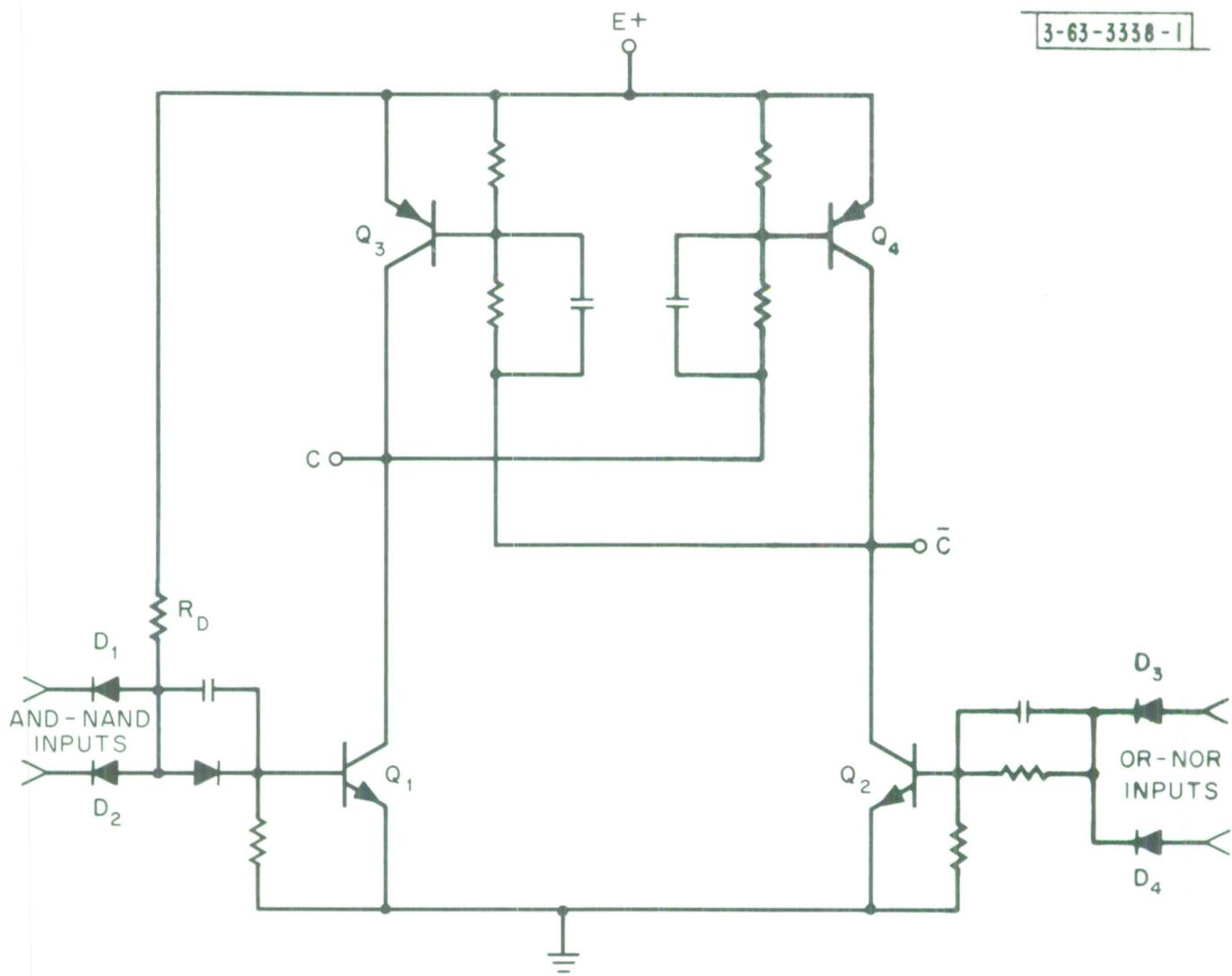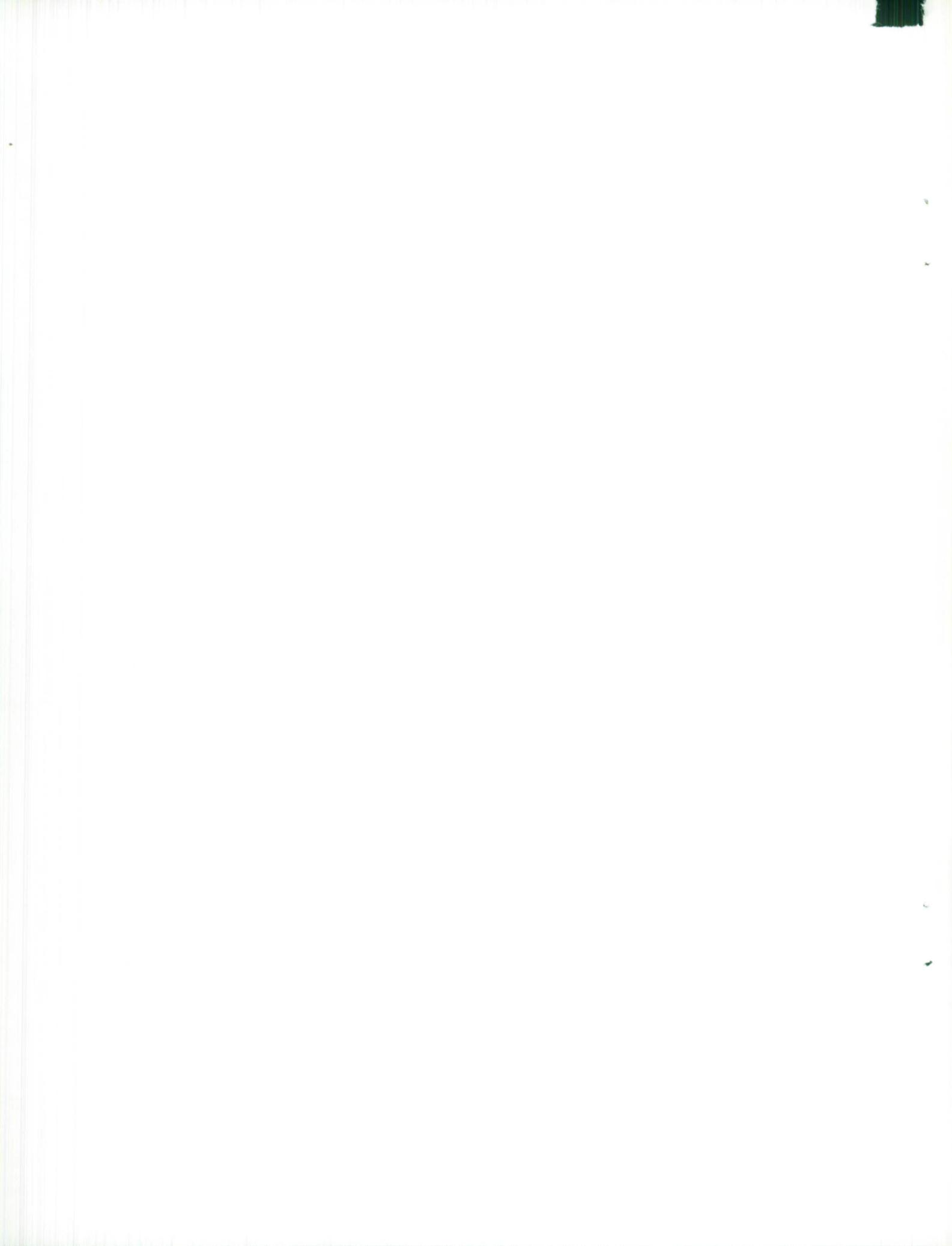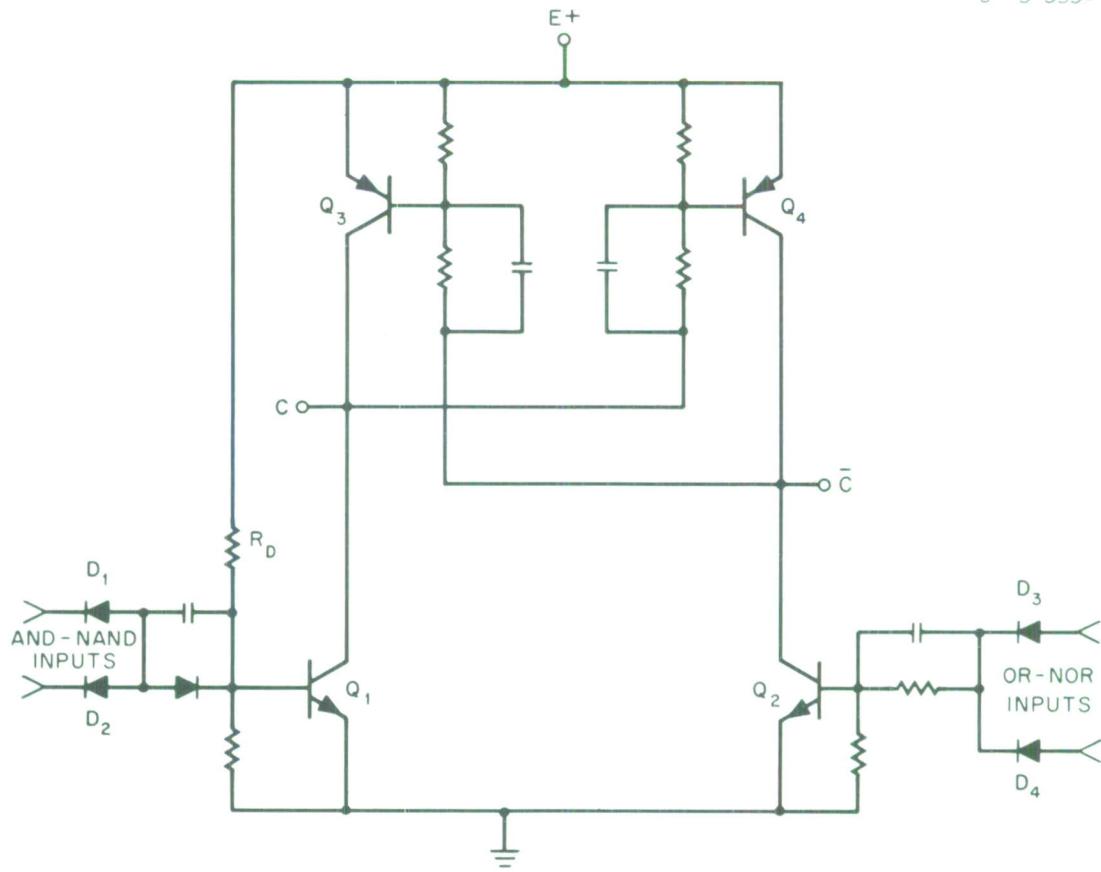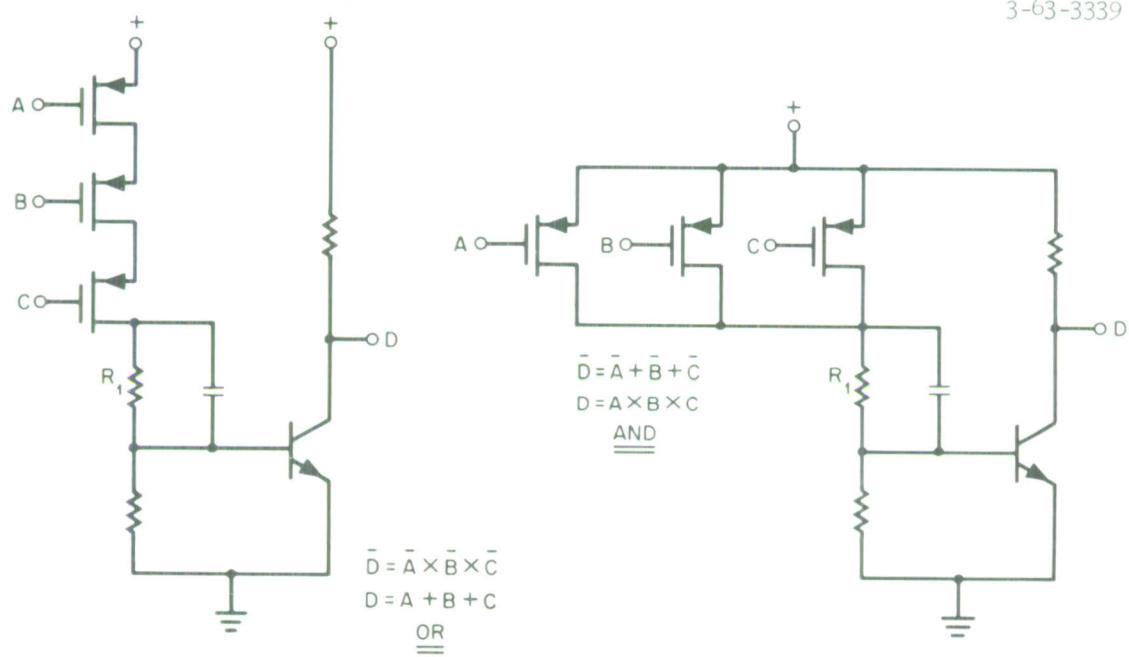
3-63-3340
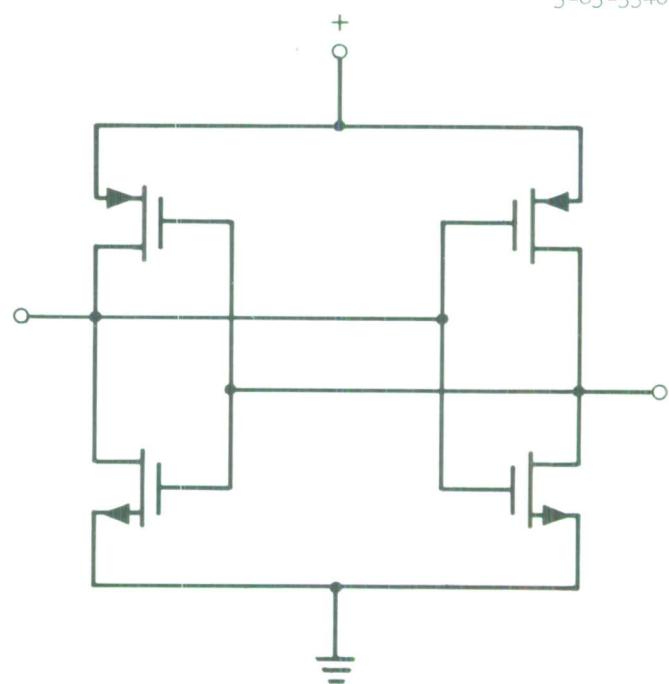
Fig. 17

DISTRIBUTION LIST

Division 6

G. P. Dinneen
W. E. Morrow
R. T. Prosser
S. Gould

Group 63

H. Sherman
R. M. Lerner
D. C. MacLellan
P. Waldron
R. S. Berg
C. Burrowes
M. C. Crocker
J. P. Densler
A. I. Grayzel
P. V. Lambert
C. L. Mack
R. E. McMahon
L. D. Michelove
J. L. Ryan
F. W. Sarles
W. G. Schmidt
I. I. Shapiro
L. V. Slocum
D. M. Snider
A. G. Stanley
L. J. Travis
N. R. Trudeau
E. A. Vrablik

DOCUMENT CONTROL DATA – DD 1473

1. ORIGINATING ACTIVITY	2a. REPORT CLASSIFICATION
Lincoln Laboratory, M.I.T.	Uncl.
	2b. DOWNGRADING GROUP

3. REPORT TITLE

Design Aspects of Minimal-Power Digital Circuitry

4. TYPE OF REPORT AND INCLUSIVE DATES
Group Report

5. AUTHOR(S) *(Last name first)*

Schmidt, W. G. and Chace, D. E.

6. REPORT DATE	7a. NO. OF PAGES	7b. NO. OF REFS.
9 February 1965	38	3

8a. CONTRACT NO.	9a. ORIGINATOR'S REPORT NO.
AF 19(628)-500	Group Report 1965-6
8b. ORDER NO.	9b. OTHER REPORT NO(S).
None	ESD-TDR-65-45

10. AVAILABILITY OR LIMITATION NOTICES

11. SUPPLEMENTARY NOTES	12. SPONSORING ACTIVITY
None	ESD

13. ABSTRACT

Minimal-power digital circuitry, while a necessity for spacecraft operation, has advantages which apply to both space-borne and ground-based digital data processing.

This report is a compendium of some of the low-power digital circuit design efforts in which Lincoln Laboratory has been engaged for the past few years. These techniques have been employed in a number of scientific satellites and space probes; similar designs are to be used in the Lincoln Experimental Satellite (LES).

The report concludes with a discussion of the influence of new semiconductor devices upon the minimal-power concept.

14. KEY WORDS

circuits and components
LES
semiconductors